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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/894,400	06/28/2001	Young-kyun Cho	8021-57- (SS-15453-US)	6437

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F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
ZHENG, EVA Y	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 11/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/894,400	CHO, YOUNG-KYUN	
	Examiner	Art Unit	
	Eva Yi Zheng	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-9,13 and 15-17* is/are rejected.

7)☒ Claim(s) *2-4,10-12,14 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 13 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen (US 5,850,422).

a) Regarding claim 13, Chen discloses a program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for recovering a clock signal in a communications system comprising a transmitter and receiver, the method steps comprising:

receiving a receiver clock signal (30 in Fig. 2) of the receiver having a frequency equal to the frequency of a transmitter clock signal of the transmitter (Col 4, L 14-16), and generating a plurality of phase clock signals (12 in Fig. 1) from the receiver clock signal, wherein each phase clock signal has the same frequency as the receiver clock signal and a different phase offset from the phase of the receiver clock signal (Col 3, L62 – Col 4, L2);

detecting a phase difference (18 in Fig. 1) between data received from the transmitter (36 in Fig. 1) and a recovery clock signal (48 in Fig. 1) and generating a first control signal indicative of a detected phase difference (as shown in Fig. 1);

outputting a second control signal from a bidirectional shift register (20 in Fig. 1; Col 3, L34-36) in response to the first control signal; and

selecting one of the plurality of phase clock signals in response to the second control signal (16 in Fig. 1) and outputting the selected phase clock signal as a recovery clock signal (48 in Fig. 1; Col 5, L 8-12).

b) Regarding claim 16, Chen discloses a communications system, comprising:

a transmitter (Col 7, L11-13); and

a receiver (Col 7, L11-13) comprising means for recovering a clock signal (10 in Fig. 1), wherein the means for recovering a clock signal comprises:

phase detecting means (18 in Fig. 1) for detecting a phase difference between data received from the transmitter (36 in Fig. 1) and a recovery clock signal (48 in Fig. 1) and generating a first control signal indicative of a detected phase difference(as shown in Fig. 1) ;

bidirectional shift register (20 in Fig. 1; Col 3, L34-36) means for outputting a second control signal in response to the first control signal;

multiphase clock signal generating means (12 in Fig. 1) for generating a plurality of phase clock signals each having the same frequency as a receiver clock signal of the receiver and a different phase offset from the phase of the receiver clock signal (Col 3, L62 – Col 4, L2); and

selecting means (16 in Fig. 1) responsive to the second control signal for selecting one of the plurality of phase clock signals (P0-P9 in Fig. 1) and outputting the selected phase clock signal as a recovery clock signal (48 in Fig. 1; Col 5, L 8-12).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 5-9, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 5,850,422) in view of Applicant Admitted Prior Art (AAPR).

a) Regarding claim 1, Chen discloses a circuit for recovering a clock signal in a receiver, the circuit comprising:

a phase detector (18 in Fig. 1) for detecting a phase difference between data received from a transmitter (36 in Fig. 1) and a recovery clock signal (48 in Fig. 1) and generating a first control signal indicative of a detected phase difference (as shown in Fig. 1);

a bidirectional shift register (20 in Fig. 1; Col 3, L34-36) for outputting a second control signal in response to the first control signal;

a multiphase clock signal generator (12 in Fig. 1) for processing a receiver clock signal of the receiver, wherein the receiver clock signal is the same as a transmitter clock signal of the transmitter (Col 4, L 14-16), to generate a plurality of phase clock signals each having the same frequency as the receiver clock signal and a different phase offset from the phase of the receiver clock signal (Col 3, L62 – Col 4, L2); and

a phase selector (16 in Fig. 1) responsive to the second control signal for selecting one of the plurality of phase clock signals and outputting the selected phase clock signal as a recovery clock signal (48 in Fig. 1; Col 5, L 8-12).

Chen discloses all the subjects described above, except for explicitly teaching of a Universal serial bus (USB) transmitter and receiver for recovering clock signals.

However, Chen's invention is for a high-speed serial interface clock/data recovery. Serial interface standards are used for improvement of I/O performance of a computer system or network (Col 1, L7-12). A USB is an interface standard for peripheral devices of a personal computer system (present application background).

A USB is a well-known communication interface standard. To recover data transmitted form a USB transmitter, the USB receiver must recover a clock signal having the same frequency and phase as the clock of the USB transmitter (present application background). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to adapt a USB transceiver in Chen's clock signal recover system for better signal recovery accuracy. And by doing so, reduce circuitry size, reduce power consumption, and recover signal within a short period of time.

b) Regarding claim 9, Chen discloses a method for recovering a clock signal in a receiver, the method comprising the steps of:

receiving a receiver clock signal (30 in Fig. 2) of the receiver having a frequency equal to the frequency of a transmitter clock signal of a transmitter (Col 4, L 14-16), and generating a plurality of phase clock signals (12 in Fig. 1) from the receiver clock signal, wherein each phase clock signal has the same frequency as the receiver clock signal and a different phase offset from the phase of the receiver clock signal (Col 3, L62 – Col 4, L2);

detecting a phase difference (18 in Fig. 1) between data received from the transmitter (36 in Fig. 1) and a recovery clock signal (48 in Fig. 1) and generating a first control signal indicative of a detected phase difference (as shown in Fig. 1);

outputting a second control signal from a bidirectional shift register (20 in Fig. 1; Col 3, L34-36) in response to the first control signal; and

selecting one of the plurality of phase clock signals in response to the second control signal (16 in Fig. 1) and outputting the selected phase clock signal as a recovery clock signal (48 in Fig. 1; Col 5, L 8-12).

Chen discloses all the subjects described above, except for explicitly teaching of a Universal serial bus (USB) transmitter and receiver for recovering clock signals.

However, Chen's invention is for a high-speed serial interface clock/data recovery. Serial interface standards are used for improvement of I/O performance of a computer system or network (Col 1, L7-12). A USB is an interface standard for peripheral devices of a personal computer system (present application background).

A USB is a well-known communication interface standard. To recover data transmitted form a USB transmitter, the USB receiver must recover a clock signal having the same frequency and phase as the clock of the USB transmitter (present application background). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to adapt a USB transceiver in Chen's clock signal recover system for better signal recovery accuracy. And by doing so, reduce circuitry size, reduce power consumption, and recover signal within a short period of time.

c) Regarding claim 5, Chen discloses the circuit of claim 1, wherein the bidirectional shift register is shifted in a first direction when the first control signal is at a first

predetermined level, and shifted in a second direction when the first control signal is at a second predetermined level (Col 6, L45-49).

d) Regarding claim 6, Chen discloses the circuit of claim 1, wherein the multiphase clock signal generator comprises a multiphase analog PLL circuit (12 in Fig. 1; more detailed circuitry shown in Fig. 2)

e) Regarding claim 7, Chen discloses the circuit of claim 1, further comprising a clocks signal generator for generating the receiver clock signal (inherent as reference signal, as shown 34 in Fig. 2).

f) Regarding claim 8, Chen discloses the circuit according to claim 7, wherein the clock signal generator comprises:

a crystal oscillator (30 in Fig.2) for generating a clock signal having a predetermined frequency; and

a frequency multiplier (32 in Fig. 2) for multiplying the frequency of the clock signal to generate the receiver clock signal.

g) Regarding claims 15 and 17, Chen discloses all the subjects described above, except for explicitly teaching of a Universal serial bus (USB) transmitter and receiver for recovering clock signals.

However, Chen's invention is for a high-speed serial interface clock/data recovery. Serial interface standards are used for improvement of I/O performance of a computer system or network (Col 1, L7-12). A USB is an interface standard for peripheral devices of a personal computer system (present application background).

A USB is a well-known communication interface standard. To recover data transmitted form a USB transmitter, the USB receiver must recover a clock signal

having the same frequency and phase as the clock of the USB transmitter (present application background). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to adapt a USB transceiver in Chen's clock signal recover system for better signal recovery accuracy. And by doing so, reduce circuitry size, reduce power consumption, and recover signal within a short period of time.

Allowable Subject Matter

5. Claims 2-4, 10-12, 14 and 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Yi Zheng whose telephone number is (571) 272-3049. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-879-9306.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Eva Yi Zheng
Examiner
Art Unit 2634

October 20, 2004

SHUWANG LIU
PRIMARY EXAMINER